

NLAST4599

Low Voltage Single Supply SPDT Analog Switch

The NLAST4599 is an advanced high speed CMOS single pole – double throw analog switch fabricated with silicon gate CMOS technology. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This switch controls analog and digital voltages that may vary across the full power–supply range (from V_{CC} to GND).

The device has been designed so the ON resistance (R_{ON}) is much lower and more linear over input voltage than R_{ON} of typical CMOS analog switches.

The channel select input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- Select Pin Compatible with TTL Levels
- Channel Select Input Over–Voltage Tolerant to 5.5 V
- Fast Switching and Propagation Speeds
- Break–Before–Make Circuitry
- Low Power Dissipation: $I_{CC} = 2 \mu A$ (Max) at $T_A = 25^\circ C$
- Diode Protection Provided on Channel Select Input
- Improved Linearity and Lower ON Resistance over Input Voltage
- Latch–up Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; MM > 200 V
- Chip Complexity: 38 FETs
- Pb–Free Packages are Available

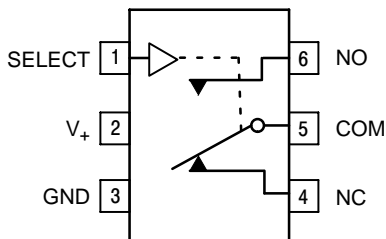


Figure 1. Pin Assignment

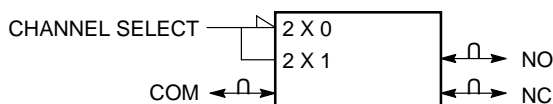


Figure 2. Logic Symbol



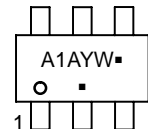
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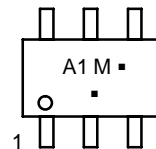
MARKING DIAGRAMS



TSOP-6
DT SUFFIX
CASE 318G



SC-88/SC-70/SOT-363
DF SUFFIX
CASE 419B



- A1 = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- M = Date Code*
- = Pb–Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position and underbar may vary depending upon manufacturing location.

FUNCTION TABLE

Select	ON Channel
L	NC
H	NO

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Positive DC Supply Voltage	V_{CC}	-0.5 to +7.0	V
Analog Input Voltage (V_{NO} or V_{COM})	V_{IS}	$-0.5 \leq V_{IS} \leq V_{CC} + 0.5$	V
Digital Select Input Voltage	V_{IN}	$-0.5 \leq V_I \leq +7.0$	V
DC Current, Into or Out of Any Pin	I_{IK}	± 50	mA
Power Dissipation in Still Air	P_D	200 200	mW
	SC-88 TSOP6		
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature, 1mm from Case for 10 seconds	T_L	260	°C
Junction Temperature Under Bias	T_J	150	°C
ESD Withstand Voltage	V_{ESD}	2000 200 N/A	V
	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)		
Latchup Performance	$I_{LATCHUP}$	± 300	mA
	Above V_{CC} and Below GND at 125°C (Note 5)		
Thermal Resistance	θ_{JA}	333 333	°C/W
	SC-88 TSOP6		

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
- Tested to EIA/JESD22-A114-A
- Tested to EIA/JESD22-A115-A
- Tested to JESD22-C101-A
- Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
DC Supply Voltage	V_{CC}	2.0	5.5	V
Digital Select Input Voltage	V_{IN}	GND	5.5	V
Analog Input Voltage (NC, NO, COM)	V_{IS}	GND	V_{CC}	V
Operating Temperature Range	T_A	-55	+125	°C
Input Rise or Fall Time SELECT	t_r, t_f	0 0	100 20	ns/V
	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$			

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

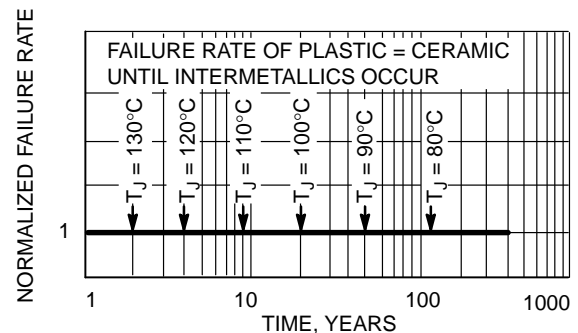


Figure 3. Failure Rate vs. Time Junction Temperature

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DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Parameter	Condition	Symbol	V _{CC}	Guaranteed Limit			Unit
				-55 to 25°C	<85°C	<125°C	
Minimum High-Level Input Voltage, Select Input		V _{IH}	3.0	2.0	2.0	2.0	V
			4.5	2.0	2.0	2.0	
			5.5	2.0	2.0	2.0	
Maximum Low-Level Input Voltage, Select Input		V _{IL}	3.0	0.5	0.5	0.5	V
			4.5	0.8	0.8	0.8	
			5.5	0.8	0.8	0.8	
Maximum Input Leakage Current, Select Input	V _{IN} = 5.5 V or GND	I _{IN}	5.5	±0.1	±1.0	±1.0	µA
Power Off Leakage Current	V _{IN} = 5.5 V or GND	I _{OFF}	0	±10	±10	±10	µA
Maximum Quiescent Supply Current	Select and V _{IS} = V _{CC} or GND	I _{CC}	5.5	1.0	1.0	2.0	µA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Parameter	Condition	Symbol	V _{CC}	Guaranteed Limit			Unit
				-55 to 25°C	<85°C	<125°C	
Maximum "ON" Resistance (Figures 17 – 23)	V _{IN} = V _{IL} or V _{IH} V _{IS} = GND to V _{CC} I _{IN} ≤ 10.0 mA	R _{ON}	2.5	85	95	105	Ω
			3.0	45	50	55	
			4.5	30	35	40	
			5.5	25	30	35	
ON Resistance Flatness (Figures 17 – 23)	V _{IN} = V _{IL} or V _{IH} I _{IN} ≤ 10.0 mA V _{IS} = 1V, 2V, 3.5V	R _{FLAT} (ON)	4.5	4	4	5	Ω
ON Resistance Match Between Channels	V _{IN} = V _{IL} or V _{IH} I _{IN} ≤ 10.0 mA V _{NO} or V _{NC} = 3.5 V	ΔR _{ON} (ON)	4.5	2	2	3	Ω
NO or NC Off Leakage Current (Figure 9)	V _{IN} = V _{IL} or V _{IH} V _{NO} or V _{NC} = 1.0 V _{COM} 4.5 V	I _{NC(OFF)} I _{NO(OFF)}	5.5	1	10	100	nA
COM ON Leakage Current (Figure 9)	V _{IN} = V _{IL} or V _{IH} V _{NO} 1.0 V or 4.5 V with V _{NC} floating or V _{NO} 1.0 V or 4.5 V with V _{NO} floating V _{COM} = 1.0 V or 4.5 V	I _{COM(ON)}	5.5	1	10	100	nA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Parameter	Test Conditions	Symbol	V_{CC} (V)	V_{IS} (V)	Guaranteed Max Limit						Unit	
					-55 to 25°C			<85°C		<125°C		
					Min	Typ*	Max	Min	Max	Min		Max
Turn-On Time (Figures 12 and 13)	$R_L = 300 \Omega$, $C_L = 35$ pF (Figures 5 and 6)	t_{ON}	2.5	2.0	5	23	28	5	30	5	30	ns
			3.0	2.0	5	16	21	5	25	5	25	
			4.5	3.0	2	11	16	2	20	2	20	
			5.5	3.0	2	9	14	2	20	2	20	
Turn-Off Time (Figures 12 and 13)	$R_L = 300 \Omega$, $C_L = 35$ pF (Figures 5 and 6)	t_{OFF}	2.5	2.0	1	7	12	1	15	1	15	ns
			3.0	2.0	1	5	10	1	15	1	15	
			4.5	3.0	1	4	9	1	12	1	12	
			5.5	3.0	1	3	8	1	12	1	12	
Minimum Break-Before-Make Time	$V_{IS} = 3.0$ V (Figure 4) $R_L = 300 \Omega$, $C_L = 35$ pF	t_{BBM}	2.5	2.0	1	12		1		1		ns
			3.0	2.0	1	11		1		1		
			4.5	3.0	1	6		1		1		
			5.5	3.0	1	5		1		1		
Typical @ 25, $V_{CC} = 5.0$ V												
Maximum Input Capacitance, Select Input Analog I/O (switch off) Common I/O (switch off) Feedthrough (switch on)		C_{IN} C_{NO} or C_{NC} C_{COM} $C_{(ON)}$						8 10 10 20			pF	

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

Parameter	Condition	Symbol	V_{CC} V	Typical 25°C	Unit
Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response (Figure 10)	$V_{IN} = 0$ dBm V_{IN} centered between V_{CC} and GND (Figure 7)	BW	3.0 4.5 5.5	170 200 200	MHz
Maximum Feedthrough On Loss	$V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 7)	V_{ONL}	3.0 4.5 5.5	-2 -2 -2	dB
Off-Channel Isolation (Figure 10)	$f = 100$ kHz; $V_{IS} = 1$ V RMS V_{IN} centered between V_{CC} and GND (Figure 7)	V_{ISO}	3.0 4.5 5.5	-93 -93 -93	dB
Charge Injection Select Input to Common I/O (Figure 15)	$V_{IN} = V_{CC}$ to GND, $F_{IS} = 20$ kHz $t_r = t_f = 3$ ns $R_{IS} = 0 \Omega$, $C_L = 1000$ pF $Q = C_L * \Delta V_{OUT}$, (Figure 8)	Q	3.0 5.5	1.5 3.0	pC
Total Harmonic Distortion THD + Noise (Figure 14)	$F_{IS} = 20$ Hz to 100 kHz, $R_L = R_{gen} = 600 \Omega$, $C_L = 50$ pF $V_{IS} = 5.0$ V _{PP} sine wave	THD	5.5	0.1	%

ORDERING INFORMATION

Device	Device Nomenclature					Package	Shipping†
	Circuit Indicator	Technology	Device Function	Package Suffix	Tape & Reel Suffix		
NLAST4599DFT2	NL	AS	4599	DF	T2	SC-88/SC-70/SOT-363	3000/Tape & Reel
NLAST4599DFT2G						SC-88/SC-70/SOT-363 (Pb-Free)	
NLAST4599DTT1				DT	T1	TSOP-6	
NLAST4599DTT1G						TSOP-6 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

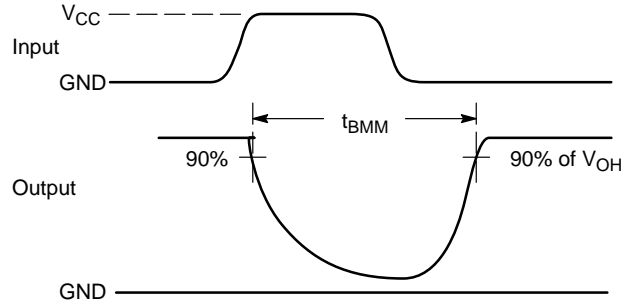
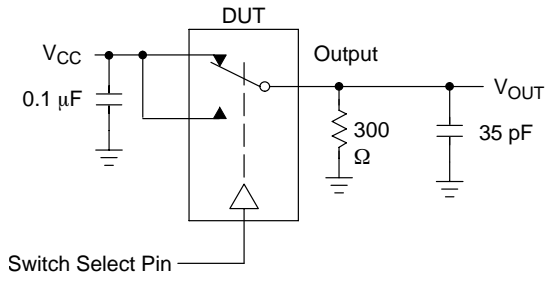


Figure 4. t_{BMM} (Time Break-Before-Make)

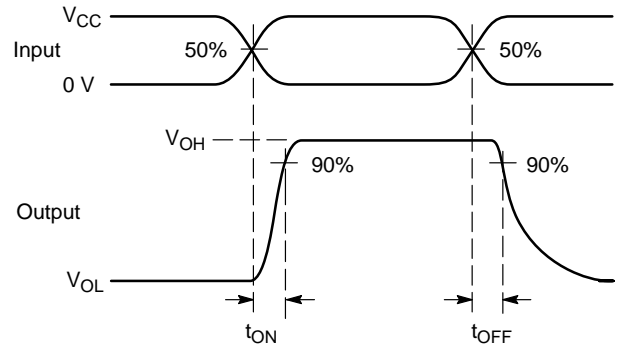
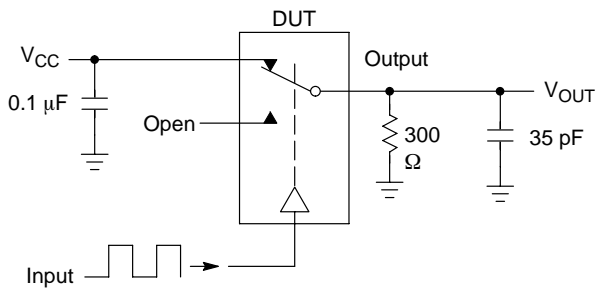


Figure 5. t_{ON}/t_{OFF}

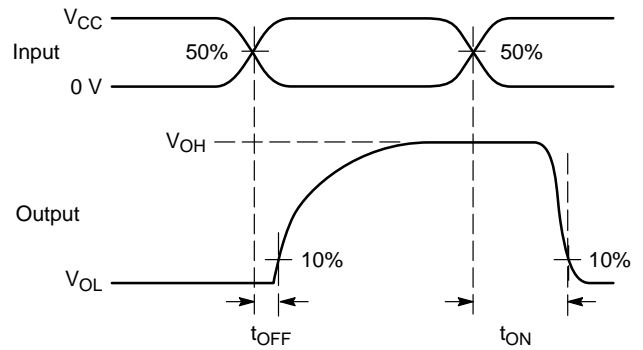
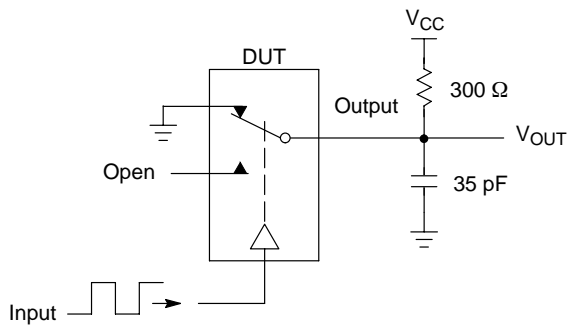
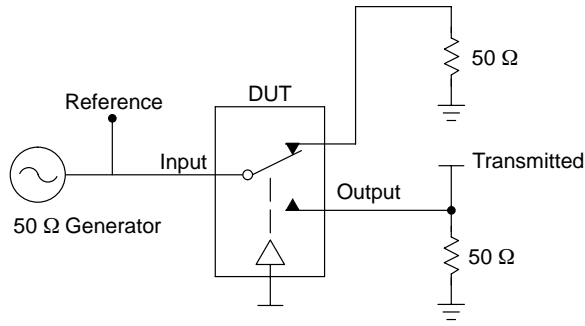


Figure 6. t_{ON}/t_{OFF}

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Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

Figure 7. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

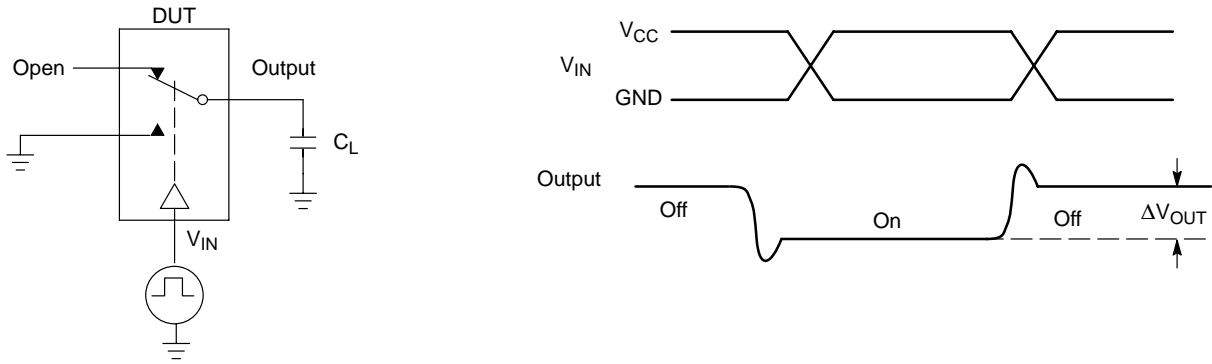


Figure 8. Charge Injection: (Q)

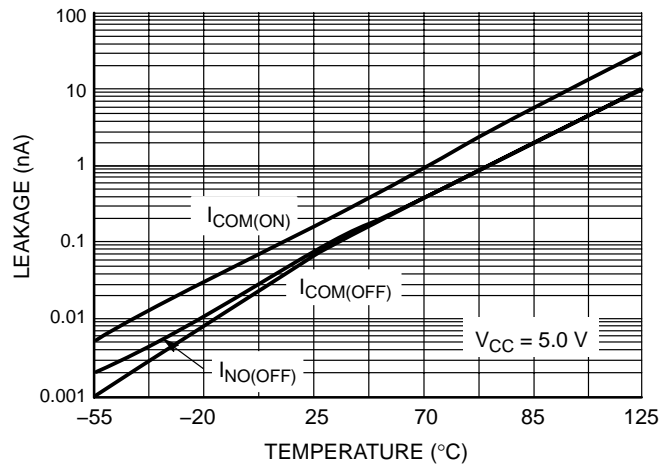


Figure 9. Switch Leakage vs. Temperature

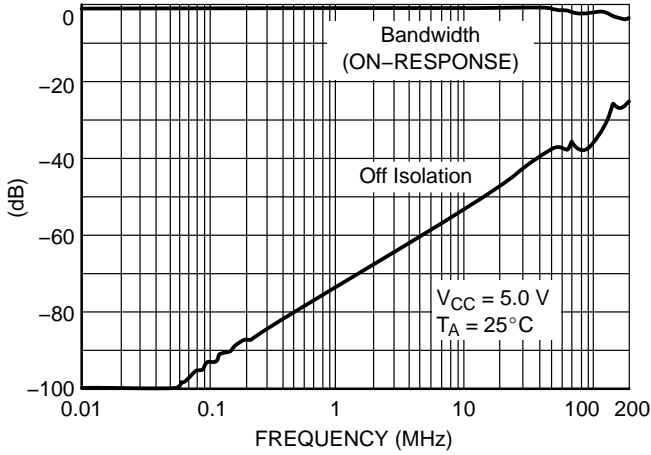


Figure 10. Bandwidth and Off-Channel Isolation

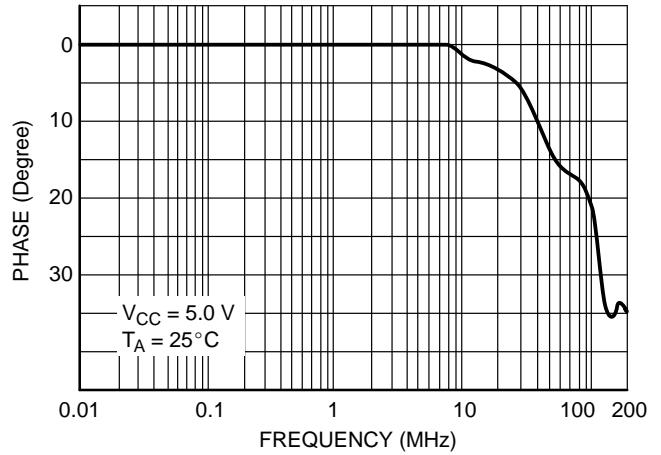


Figure 11. Phase vs. Frequency

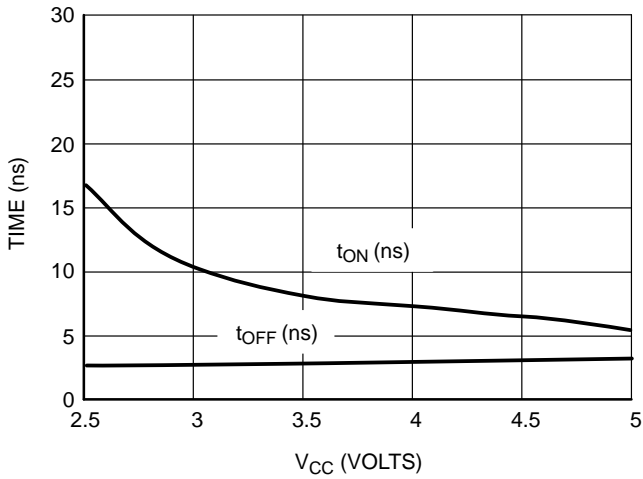


Figure 12. t_{ON} and t_{OFF} vs. V_{CC} at 25°C

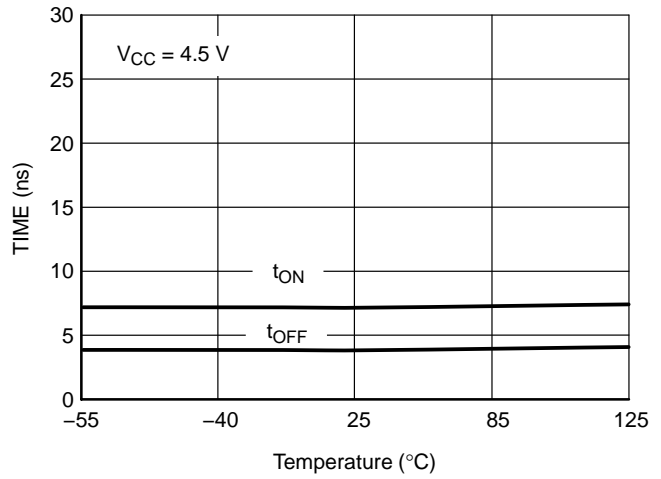


Figure 13. t_{ON} and t_{OFF} vs. Temp

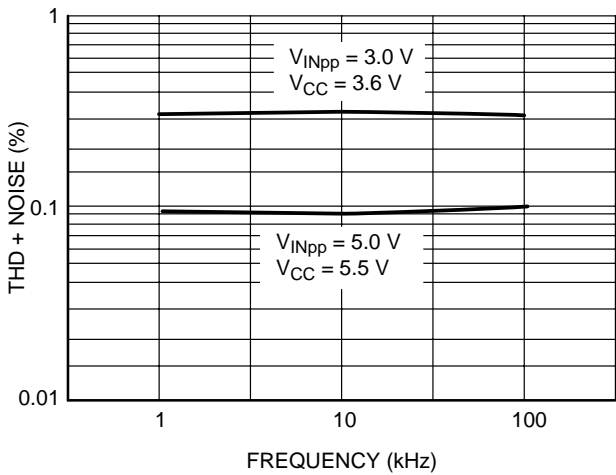


Figure 14. Total Harmonic Distortion Plus Noise vs. Frequency

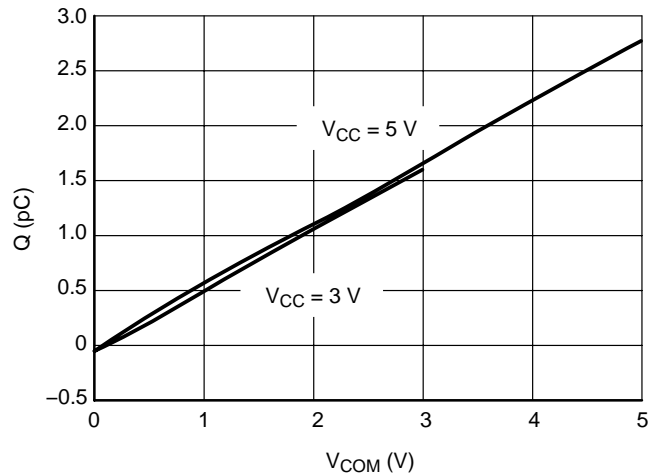


Figure 15. Charge Injection vs. COM Voltage

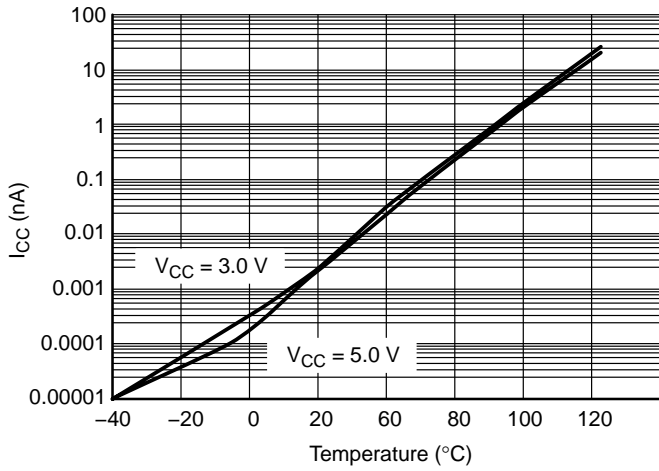


Figure 16. I_{CC} vs. Temp, $V_{CC} = 3\text{ V}$ & 5 V

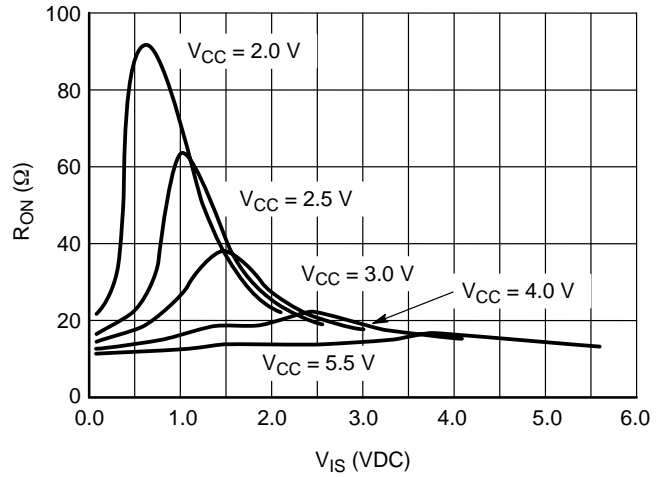


Figure 17. R_{ON} vs. V_{CC} , Temp = 25°C

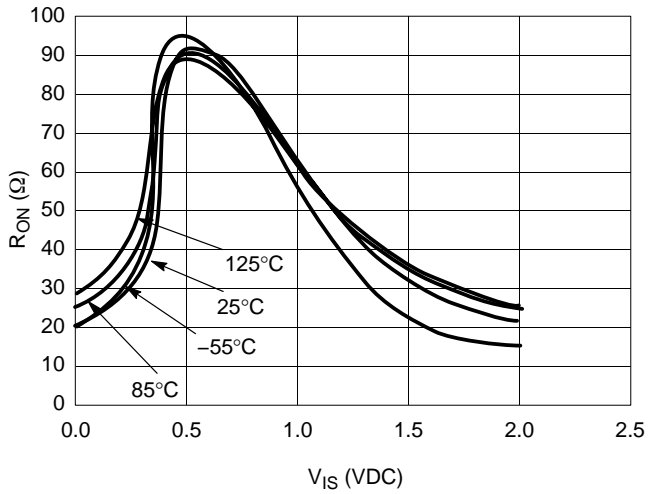


Figure 18. R_{ON} vs Temp, $V_{CC} = 2.0\text{ V}$

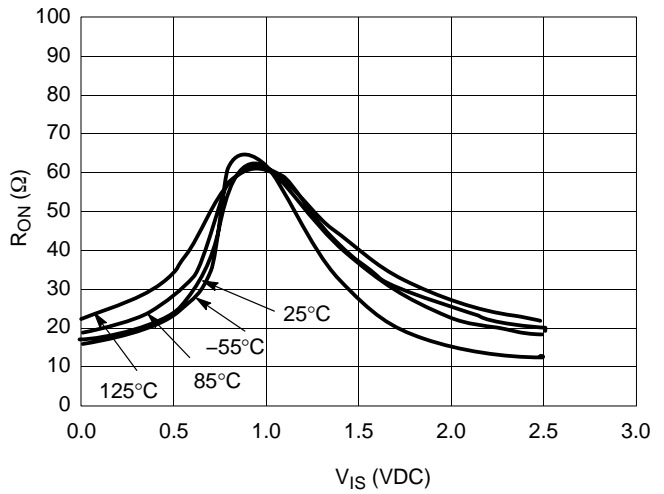


Figure 19. R_{ON} vs. Temp, $V_{CC} = 2.5\text{ V}$

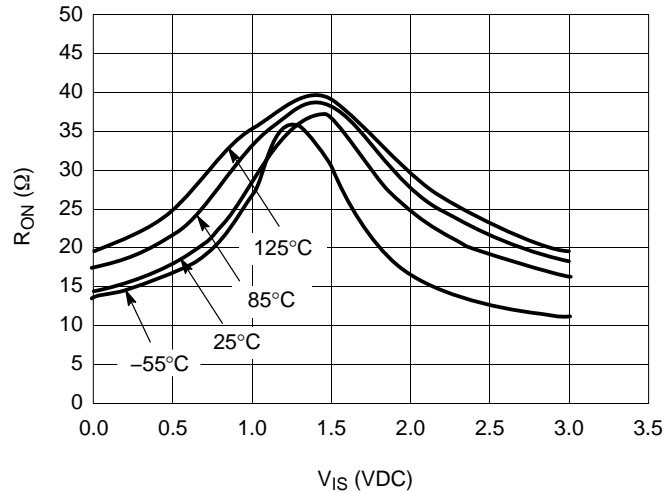


Figure 20. R_{ON} vs. Temp, $V_{CC} = 3.0\text{ V}$

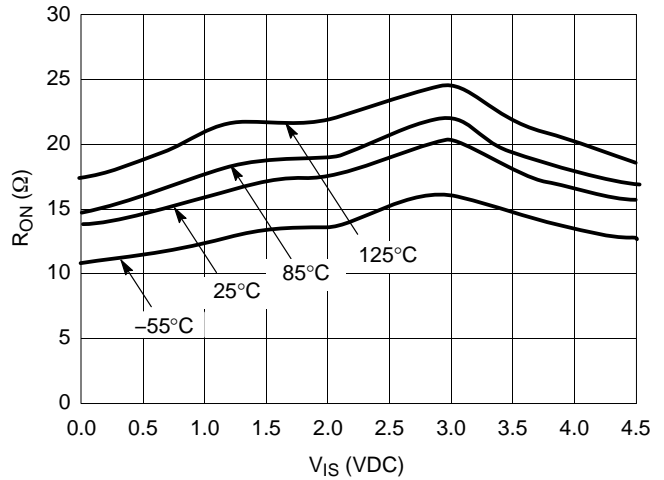


Figure 21. R_{ON} vs. Temp, $V_{CC} = 4.5\text{ V}$

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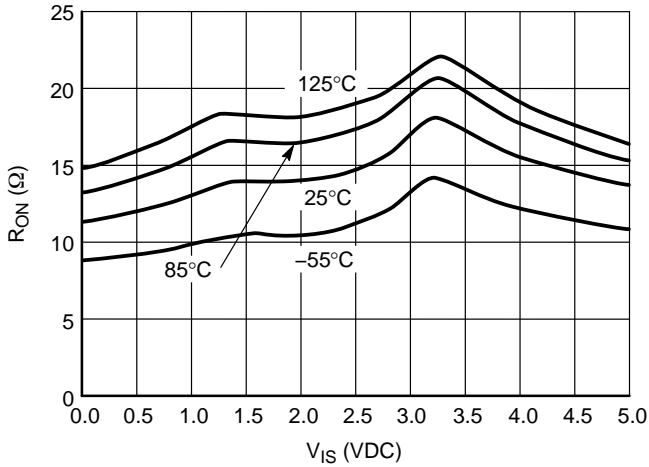


Figure 22. R_{ON} vs. Temp, $V_{CC} = 5.0$ V

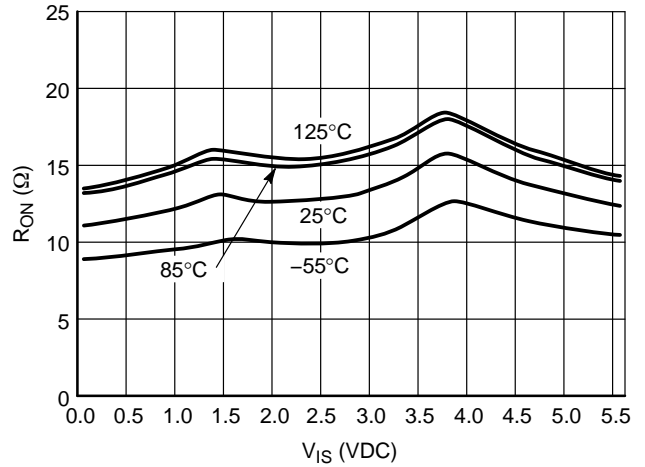


Figure 23. R_{ON} vs. Temp, $V_{CC} = 5.5$ V

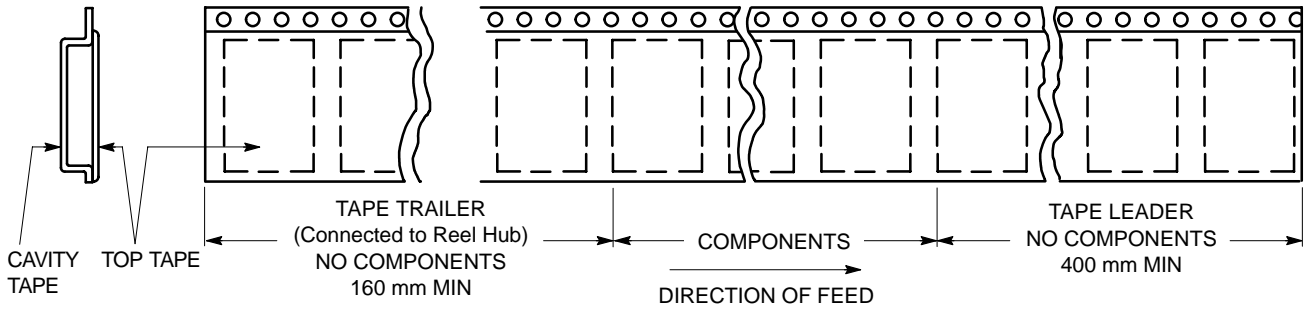


Figure 24. Tape Ends for Finished Goods

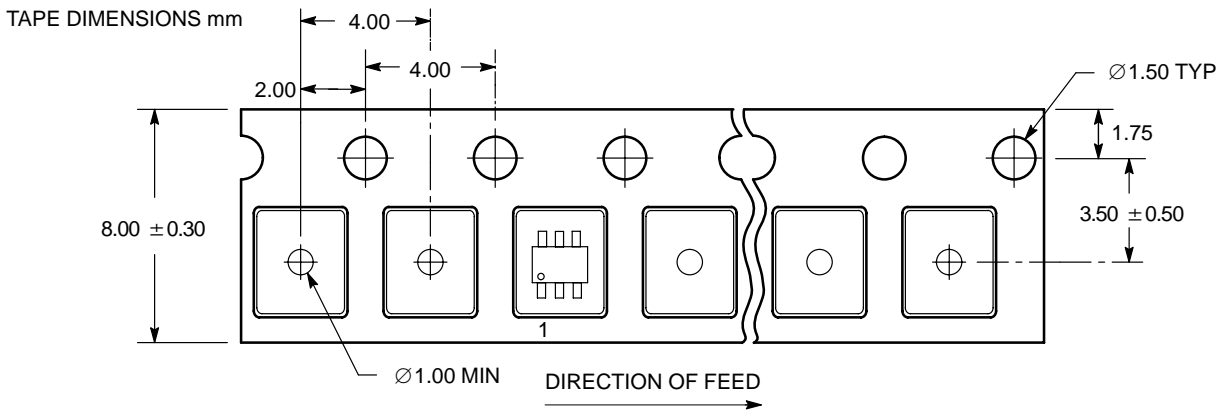


Figure 25. SC70-6/SC-88/SOT-363 DFT2 and SOT23-6/TSOP-6/SC59-6 DTT1 Reel Configuration/Orientation

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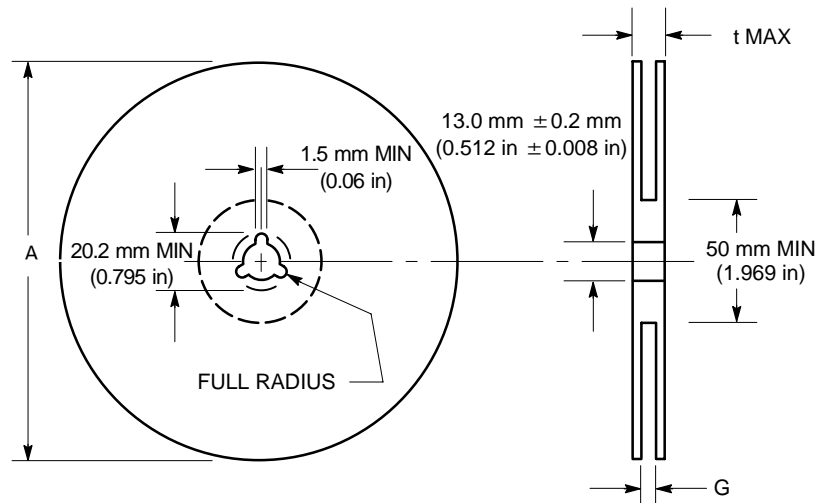


Figure 26. Reel Dimensions

REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	T1, T2	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

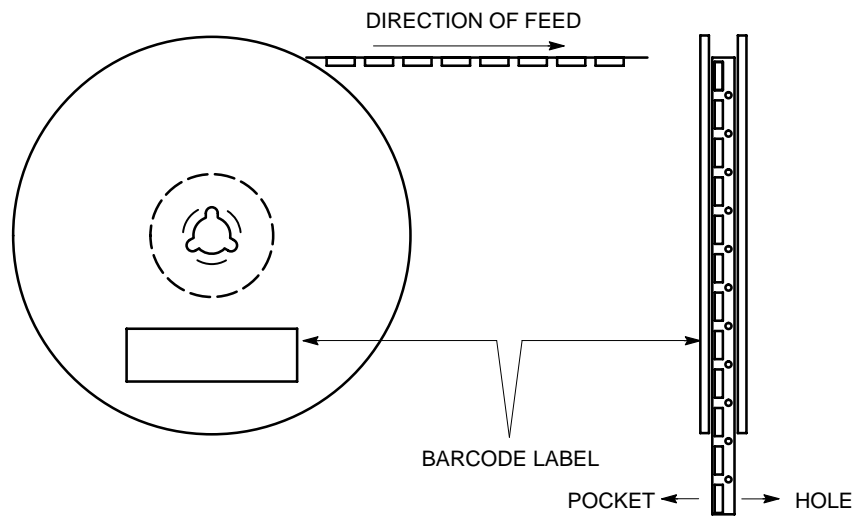
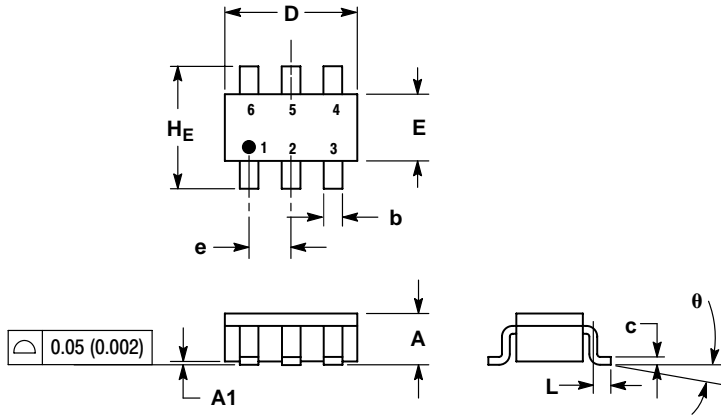


Figure 27. Reel Winding Direction

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PACKAGE DIMENSIONS

TSOP-6
CASE 318G-02
ISSUE S

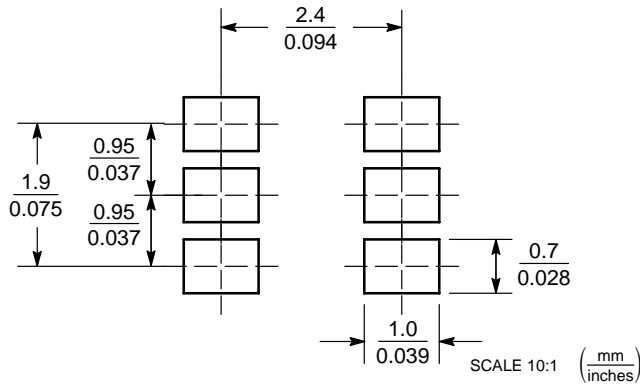


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

SOLDERING FOOTPRINT*

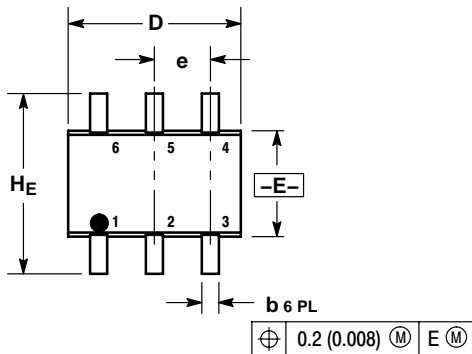


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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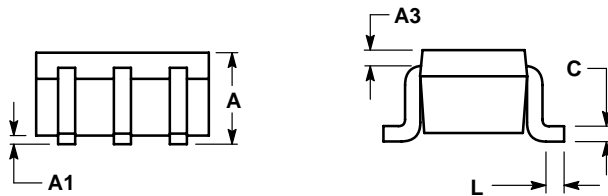
PACKAGE DIMENSIONS

SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE W

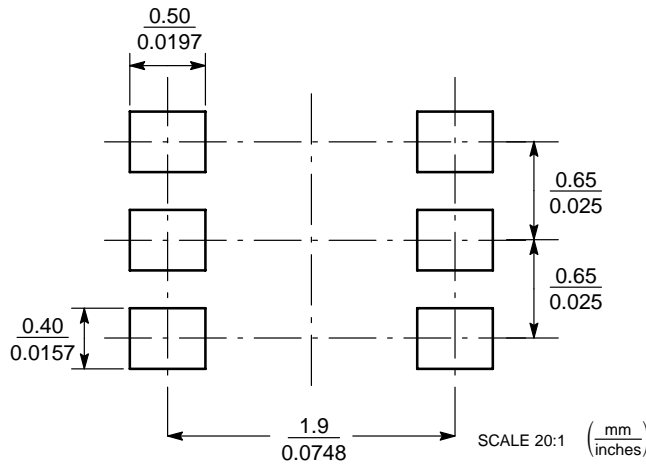


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 419B-01 OBSOLETE, NEW STANDARD 419B-02.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
HE	2.00	2.10	2.20	0.078	0.082	0.086



SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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